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LEOPARDLOGIC

CONFIGURABLE CAPABILITY FOR COMMUNICATIONS



Introduction

Welcome to Leopard Logic, Inc, the standard in Programmable IP for the communications infrastructure in the 21st Century.

In this site, you can browse our product offering, contact us, and run our tools to design you devices and systems based on Leopard Logic technology.

We are a Pre-IPO company in an exciting new area of silicon technology. Leopard Logic, Inc committed to customer satisfaction. We welcome your feedback on our technology, software and suggestions on how this web site can better serve your needs. Further detailed technical support of our technology and tools is available upon request.

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Our Mission

Deliver Required Configurable Capability for Next Generation Communication Platforms in Communication Infrastructure and the Network Access Markets to

- Provide high integration and customizable embedded configurable IP blocks
- Enable flexible low risk solutions for high growth communication and digital convergence applications
- Enable fast time to market solutions via readily accessible, easy to use, and fully integrate tools

Our Target Customer

Our technology is applicable for any ASIC SoC design that requires flexibility, low power, low and minimum risk for a fast time to revenue solution. This solution is most applicable to customers in the communications target market for power efficient and cost effective wireless, network protocol, and DSP centric product categories.

Market Application

A New Generation of Devices is Needed for:

- Distributed Computing and Data Access
- Faster and Smarter Communication Networks
- Evolving Communication Standards
- Targeted Internet Appliances
- Power Centric Design



Team

We at Leopard Logic believe that the single most valuable asset a company can have is the people who make up the team. Our team has a proven track record of on time and quality deliverables. We strive to create an atmosphere of innovation, learning, and results while providing respect and rewards for our team members. The founding team member's direct experience to bear on the Leopard Logic technology in terms of management, product development and delivery, and enabling corporate growth. The team consists of-

Chris Phillips - CEO & President

Dale Wong - VP of Technology

Hsin Wang - VP of Hardware

John Tobey - Director of Software

Dan Pugh - Director of Systems & Applications

Chris Phillips, CEO & President

Mr. Phillips has 20 years experience in microcontroller, microprocessors, FPGAs, and EDA tools at National Semiconductor, Summit Design, Integrated CMOS Systems, Crosspoint Solutions. He was most recently the founder and CTO at Chameleon Systems, Inc. Prior to that, he was Director of High Level Synthesis at Summit Design, Director of Advanced Architecture at Crosspoint on the innovative CrossFire FPGA family, and a contributor at National Semiconductor in the Integrated Processor Group on an effort to create a fully compatible 486 processor from clean room design to functional silicon in 15 weeks. He has 16 patents granted to date. BSEE, Cornell University 1981.

Dale Wong, Vice President of Technology

Mr. Wong has 17 years experience in Electronic Design Automation (EDA) algorithm development. He has 8 patents granted to date. Most recently, he was a founder and Software Engineer at Chameleon Systems, Inc. Prior to this, he was founder and Software Engineer at CADalyst, Inc., an EDA design consulting firm with an emphasis in FPGA technology. Wong has a proven track record of software tool development at Crosspoint Solutions, Technology, Cadence Design Systems, and American Microsystems. The delivery of EDA tools at Chameleon Systems and Crosspoint Solutions were delivered on time and with reported customer bugs. He designed and developed: segmented channel router, router, object oriented database, timing driven placement program, automatic pad placement, multi-chip partitioning system. At VLSI Technology, he was responsible for the development of

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Leopard Technology

A patent-protected Architectural Breakthrough in:

- Highest Cell Utilization
- Proprietary innovative interconnect Structure
- Best Performance per microWatt
- Seamless IP (Intellectual Property) Mapping
- Industry standard Design tool and Methodology Support

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Leopard Opportunity for Silicon in the 21st Century

- Cost Effective Configurability
- Pent-up Demand not being met by current solutions
- Power now a key Metric in addition to Performance and Cost
- Clear demand for programmability in Communications
- Requirement in Wireless and Encryption Domains of market usage
- Required Component in ASIC SoC IP based Design Methodologies

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of an Industry standard Floorplanning Tool including macro block placement, cell placement and routing estimation. BSCS, University of California at Berkeley, 1982

Hsin Wang, VP of Hardware

Mr. Wang has 16 years experience in designing and managing IC design projects. He recently was Senior Director of Hardware Engineering at Chameleon Systems. Prior to that, he is a founder and principle of SSD, Manager of Mentor Graphics' VLSI Design Center Service.

He has an extensive track record of successful IC tapeout projects such as the Chameleon CS 2112 Reconfigurable Communications Processor, i486 microcontroller, MIPS R4600, SUN Sparc and TI DSP C5x. He is widely recognized as being an expert in the areas of design and silicon layout generation.

John Tobey, Director of Software

Mr. Tobey has 20 years experience in the software industry. His experience has been in the CAD and Semiconductor industries (Cadence Design Systems, CAE Systems, Advanced Micro Devices, and Schlumberger Digital Test Systems). During the past 10 years he has specialized in the realm of FPGA Design and Algorithms while at AutoGate Logic. During his tenure at AutoGate Logic he developed custom FPGA system solutions for clients such as Gatefield, HLD Design, Vantis, DynaChip, and Actel. AutoGate Logic was acquired by Actel at the end of 1999. His education includes a BS in Computer Science from Colorado State University and an MS in Computer Engineering from Santa Clara University.

Dan Pugh, Director of Systems & Applications

Mr. Pugh has 15 years experience in wireless and wireline communications systems using a combination of FPGAs, ASICs, microprocessors, and DSPs. He was most recently a Senior Member of Technical Staff at Chameleon Systems where he worked with customers mapping wireless algorithms into the Chameleon Reconfigurable Communications Processor. Prior to that, he was a System Engineer at Applied Signal Technology where he spent 5 years as a key contributor defining next-generation reconnaissance and defense communications systems. As a Senior Engineer for Radix Technologies, Mr. Pugh designed an adaptive beamforming processing card for a fixed wireless local loop system for the military. Mr. Pugh is familiar with many standards including UMTS/3GPP, CDMA2000/3GPP, IS-95 CDMA, ATM, and PDH/SDH Multiplexers. BSEE, University of California at Berkeley, 1985. MSEE, University of California at Davis, 1987

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